Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A head-connection-polarity detector, comprising:

a circuit operable to recover servo data from a servo signal generated by a read-write head that is coupled to the circuit with a connection polarity; and

a determinator coupled to the circuit and operable to determine the connection polarity from the recovered servo data.

2. (Original) The detector of claim 1 wherein:

the circuit is operable to recover a servo-synchronization mark from the servo signal; and

the determinator is operable to determine the connection polarity from the recovered servo-synchronization mark.

3. (Original) The detector of claim 1 wherein the deteminator is operable to generate a signal that indicates the determined connection polarity.

4. (Original) The detector of claim 1 wherein the circuit comprises a Viterbi detector.

5. (Original) The detector of claim 1 wherein the circuit is operable to recover the servo data from the servo signal regardless of the connection polarity.

6. (Original) A Viterbi detector, comprising:

an input terminal operable to receive a signal that represents a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels; and

a recovery circuit coupled to the input terminal, the circuit operable to recover the binary sequence from the signal by,

calculating a respective path metric for each of no more than two possible states of the binary sequence, and

determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path.

7. (Original) The Viterbi detector of claim 6, further comprising:

a register coupled to the recovery circuit; and

wherein the recovery circuit is operable to load the recovered binary sequence into the register.

8. (Original) The Viterbi detector of claim 6 wherein:

the first logic level equals logic 1; and

the second logic level equals logic 0.

9. (Original) The Viterbi detector of claim 6 wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating a respective path metric for two and only two possible states of the binary sequence.

10. (Original) The Viterbi detector of claim 6 wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating a respective path metric for and only for possible binary states 00 and 11.

11. (Original) The Viterbi detector of claim 6 wherein the recovery circuit is operable to recover the binary sequence from the signal according to a PR4 protocol.

12. (Original) The Viterbi detector of claim 6 wherein:

the input terminal is operable to receive samples of the signal; and

the recovery circuit is operable to process two samples at a time.

13. (Original) A Viterbi detector, comprising:

an input terminal operable to receive samples of a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's; and

a recovery circuit coupled to the input terminal and to the register, the circuit operable to recover the binary sequence from the signal by,

for each pair of samples, calculating multiple path metrics for no more than two possible states of the binary sequence, and

determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path.

14. (Original) The Viterbi detector of claim 13 wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating, for each pair of samples, multiple path metrics for two of the possible binary states and only two of the possible binary states.

15. (Original) The Viterbi detector of claim 13 wherein the recovery circuit is operable to recover the binary sequence from the signal by:

for each pair of samples, calculating multiple path metrics for the possible binary states 00 and 11 and only the possible binary states 00 and 11.

16. (Original) The Viterbi detector of claim 13 wherein the recovery circuit is operable to recover the binary sequence from the signal by:

for each pair of samples, calculating no path metrics for the possible binary states 01 and 10; and

for each pair of samples, calculating two respective path metrics for each of the possible binary states 00 and 11.

17. (Original) A Viterbi detector, comprising:

an input terminal operable to receive samples of a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's; and

a recovery circuit coupled to the input terminal and to the register, the circuit operable to recover the binary sequence from the signal by,

for each pair of samples, calculating a difference between path metrics for two possible states of the binary sequence, and

determining a surviving path from the difference, the binary sequence lying along the surviving path.

18. (Original) The Viterbi detector of claim 17 wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating, for each pair of samples, the difference and only the difference between the path metrics for the two possible states.

19. (Original) The Viterbi detector of claim 17 wherein the recovery circuit is operable to recover the binary sequence from the signal by calculation, for each pair of samples, of the difference between the path metrics for the two possible states 00 and 11.

20. (Original) The Viterbi detector of claim 17 wherein the recovery circuit is operable to recover the binary sequence from the signal by:

for each pair of samples, calculating no path metrics for or difference metric between possible binary states 01 and 10; and

for each pair of samples, calculating the difference between the path metrics for possible binary states 00 and 11.

21. (Original) A synchronization-mark-and-head-connection polarity detector, comprising:

a Viterbi detector operable to recover a synchronization mark from samples of a servo signal generated by a read head that is coupled to the Viterbi detector with a connection polarity; and

a comparator coupled to the Viterbi detector and operable to determine the connection polarity from the recovered synchronization mark.

22. (Original) The detector of claim 21 wherein the comparator is operable to generate a signal that indicates the determined connection polarity.

23. (Original) The detector of claim 21 wherein the Viterbi detector is operable to recover the synchronization mark from the servo signal regardless of the connection polarity of the read head.

24. (Original) The detector of claim 21 wherein:

the synchronization mark has pairs and only pairs of consecutive logic 0's and logic 1's; and

the Viterbi detector comprises,

a recovery circuit operable to recover the synchronization mark from the samples of the servo signal by,

for each pair of samples, calculating a difference between path metrics for possible states 00 and 11 of the synchronization mark, and

determining a surviving path from the difference, the synchronization mark lying along the surviving path.

25. (Original) The detector of claim 21 wherein the comparator is operable to determine the connection polarity by:

comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis;

determining that the connection polarity equals a first polarity if the number of mismatching bits is less than or equal to a first predetermined threshold; and

determining that the connection polarity equals a second polarity if the number of mismatching bits is greater than or equal to a second predetermined threshold.

26. (Original) The detector of claim 21 wherein the comparator is operable to determine the connection polarity by:

comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis;

determining that the connection polarity is positive if the number of mismatching bits is less than or equal to a first predetermined threshold; and

determining that the connection polarity is negative if the number of mismatching bits is greater than or equal to a second predetermined threshold.

27. (Currently Amended) A servo channel, comprising:

a sampling circuit coupled to <u>receive</u> and operable to generate samples of a servo signal that represents a servo-synchronization mark and that has a phase; and

a synchronization-mark-and-polarity detector coupled to the sampling circuit and comprising,

a first Viterbi detector operable to recover the synchronization mark from the samples of the servo signal; and

a comparator coupled to the first Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark.

28. (Original) The servo channel of claim 27 wherein:

the comparator is coupled to the sampling circuit; and

the sampling circuit is operable to generate the samples of the servo signal having a desired phase.

29. (Original) The servo channel of claim 27 wherein:

the comparator is coupled to the sampling circuit; and

if the determined phase is opposite to a desired phase, then the sampling circuit is operable to invert the samples of the servo signal.

30. (Original) The servo channel of claim 27 wherein:

the comparator is operable to generate a phase signal that indicates the determined phase; and

the sampling circuit is coupled to the phase determinator and is operable to generate the samples of the servo signal having a desired phase in response to the phase signal.

31. (Original) The servo channel of claim 27 wherein the phase of the servo signal represents a connection polarity between the sampling circuit and a read head that generates the servo signal.

32. (Original) The servo channel of claim 27, further comprising:

wherein the servo signal also represents servo data other than the synchronization mark; and

a second Viterbi detector coupled to the sampling circuit and operable to recover the other servo data from the samples of the servo signal.

33. (Currently Amended) A servo channel, comprising:

a sampling circuit coupled to <u>receive</u> and operable to generate samples of a servo signal that represents a binary sequence that includes a servo-synchronization mark and other servo data, the servo signal having a phase; and

a detector coupled to the sampling circuit and comprising,

a Viterbi detector operable to recover the synchronization mark and the other servo data from the samples of the servo signal; and

a comparator coupled to the Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark.

34. (Original) The servo channel of claim 33 wherein:

the comparator is coupled to the sampling circuit; and

if the determined phase is opposite to a desired phase, then the sampling circuit is operable to invert the samples of the servo signal.

35. (Original) The servo channel of claim 33 wherein:

the synchronization mark and other servo data include pairs and only pairs of consecutive logic 0's and logic 1's; and

the Viterbi detector is operable to recover the synchronization mark and servo data from the samples by,

for each pair of samples, calculating a difference between path metrics for two possible states of the binary sequence, and

determining a surviving path from the difference, the binary sequence lying along the surviving path.

36. (Original) A disk-drive system, comprising:

a data-storage disk having a surface and operable to store a servo synchronization mark and other servo data;

a motor coupled to and operable to rotate the disk;

a read head operable to generate a servo signal that has a phase and that represents the synchronization mark and the other servo data;

a read-head positioning assembly operable to move the read head over the surface of the disk; and

a servo channel coupled to the read head, the servo channel comprising,

a sampling circuit operable to generate samples of the servo signal and to adust a phase of the samples to a desired value in response to a determined phase of the servo signal,

a synchronization-mark-and-coupling-polarity detector coupled to the sampling circuit and comprising,

a first Viterbi detector operable to recover the synchronization mark from the samples of the servo signal, and

a comparator coupled to the first Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark and to provide the determined phase to the sampling circuit, and

a second Viterbi detector coupled to the sampling circuit and operable to recover the other servo data from the samples of the servo signal.

37. (Original) A disk-drive system, comprising:

a data-storage disk having a surface and operable to store a servo synchronization mark and other servo data;

a motor coupled to and operable to rotate the disk;

a read head operable to generate a servo signal that has a phase and that represents the synchronization mark and the other servo data;

a read-head positioning assembly operable to move the read head over the surface of the disk; and

a servo channel coupled to the read head, the servo channel comprising,

a sampling circuit operable to generate samples of the servo signal, and

a Viterbi detector operable to recover the synchronization mark and other servo data from the samples of the servo signal regardless of the phase of the servo signal.

38. (Original) A method, comprising:

generating a servo signal with a read head, the servo signal representing servo data and having a phase that represents a connection polarity of the read head;

recovering the servo data from the servo signal; and

determining the phase of the servo signal from the recovered servo data.

39. (Original) The method of claim 38 wherein:

the servo data includes a synchronization mark;

the determining comprises determining the phase of the servo signal from the recovered synchronization mark.

40. (Original) The method of claim 38, further comprising generating a signal that indicates the determined phase of the servo signal.

41. (Original) The method of claim 38, further comprising adjusting the phase of the servo signal to a desired value if the determined phase has an undesired value.

42. (Original) The method of claim 38, further comprising:

wherein the servo data includes a synchronization mark; and

the determining comprises,

comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis,

determining that the servo signal is in phase if the number of mismatching bits is less than or equal to a first predetermined threshold, and

determining that the servo signal is out of phase if the number of mismatching bits is greater than or equal to a second predetermined threshold.

43. (Original) A method, comprising:

calculating a respective path metric for each of no more than two possible states of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels; and

determining a surviving path from the calculated path metrics, a recovered binary sequence lying along the surviving path.

44. (Original) The method of claim 43 wherein the calculating comprises calculating a respective path metric for and only for possible binary states 00 and 11 of the binary sequence.

45. (Original) A method, comprising:

sampling a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's;

for each pair of samples, calculating multiple path metrics for no more than two possible states of the binary sequence; and

determining a surviving path from the calculated path metrics, a recovered binary sequence lying along the surviving path.

46. (Original) The method of claim 45 wherein the calculating comprises, for each pair of samples:

calculating no path metrics for the possible binary statess 01 and 10; and

calculating multiple two metrics for each of the possible binary states 00 and 11.

47. (Original) A method, comprising:

sampling a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's;

for each pair of samples, calculating a difference between path metrics for two possible states of the binary sequence; and

determining a surviving path from the difference, a recovered binary sequence lying along the surviving path.

48. (Original) The method of claim 47 wherein the calculating comprises, for each pair of samples:

calculating no path metrics for or difference metric between possible binary states 01 and 10; and

calculating the difference between the path metrics for possible binary states 00 and 11.

49. (Original) A method, comprising:

sampling a servo signal having a phase; and

recovering servo data from the servo signal regardless of the phase of the servo signal.